REMARKS

This Amendment amends the title of the pending application. Claims 1-19 are currently pending in the application. In view of the comments set forth below, the Applicants respectfully urge reconsideration of the outstanding rejections and urge the Examiner to pass the claims to allowance.

I. Title

The Examiner has objected to the title as being not properly descriptive of the claimed invention. In response to this objection, the Applicants have amended to the title to attempt to make it more descriptive.

II. Rejection of Claims 1, 2 and 8-19 under 35 U.S.C. §102(e).

Claims 1, 2 and 8-19 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lin (U.S. Patent No. 6,631,452). The Applicants respectfully traverse this rejection.

A. Claims 1, 2 and 8-13

Claims 1, 2 and 8-13 are directed to a microprocessor that contains a mechanism for avoiding costly software traps for filling or spilling registers that are logically partitioned into register windows. A register window fill occurs when the registers do not hold the contents of a given register window and the contents of the register window must be transferred from storage to the registers. Conversely, a register window spill occurs when the contents of one of the register windows must be transferred into storage to make room for the contents of a new register window.

The microprocessor of claim 1, 2 and 8-13 includes registers for holding values that are logically partitioned into register windows. The microprocessor also includes a storage for storing values held on the registers of the register windows. A detector detects that one of either a register window overflow condition or a register window underflow condition is imminent. In response to the detector detecting on of these conditions being imminent, an

instruction generator generates at least one instruction to manipulate the storage to avoid a trap responsive to the condition that is detected as imminent. As such, the expensive traps associated with a spill or a fill can be avoided. In one embodiment of the present invention, spill instructions, such as those listed on page 8 of the present application are inserted by applying back pressure so that there is no need for the software trap to be triggered. Analogously, pressure may be applied to facilitate suitable fill instructions, such as those depicted in Figure 10 of the present application in this embodiment.

B. Summary of Lin

Lin is concerned with a mechanism that speculatively spills data or fills data into the registers of a register file. This approach avoids a newly activated or reactivated procedure from being blocked by a spill or fill. In some cases, the spill or fill cause the processor to stall until the spill or fill operation is complete and thus, reduces the performance of the processor. Lin seeks to speculatively perform the spill or fill when the processor has available bandwidth. As noted at column 6, lines 36-29, "For one embodiment of the invention, RSE 150 tracks the register file partition and initiates speculative load and store operations between the register file and the backing store when the processor has available bandwidth." By speculatively spilling or filling, Lin avoids the stalling of a process that must wait upon the spill or fill to complete. Lin seeks to identify periods where the processor has available bandwidth so as to optimize when the speculative spilling or filling occurs.

C. Novelty of Claims 1-2 and 8-13

Claims 1-2 and 8-13 require a detector for detecting that one of a register window overflow condition and a register window underflow condition is imminent and an instruction generator that is responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap responsive to the condition that is detected as imminent. In other words the instructions for avoiding the trap are generated only when the overflow or underflow condition is imminent. In contrast, Lin discloses that the speculative spill/fill is performed when there is available bandwidth in the processor so as to not stall the active process. This speculative spill or fill is not performed in response to a detection that the register window

overflow condition or register window underflow condition is imminent. Accordingly, the Applicants respectfully urge reconsideration of the rejection of claims 1-2 and 8-13.

Claim 2 is additionally novel over the disclosure of Lin because Lin does not disclose that the detector and the instructions generator are implemented in hardware, as required by claim 2.

D. Claims 14 and 15

Claims 14 and 15 are novel over the disclosure of Lin because they require a detector for detecting that a trap that requires an access to storage to manage register window information is imminent and an instruction generator responsive to the detector for generating at least one instruction to avoid the trap. The speculative fill or spill disclosed by Lin is performed when processor bandwidth is available as opposed to in response to the determination that a trap is imminent so that the trap may be avoided. The Applicants respectfully urge reconsideration of the rejection of claims 14 and 15.

E. Claims 16-18

Claims 16-18 are novel over the disclosure of Lin because they require a method where storage is manipulated to avoid a trap that is responsive to a spill or fill that is determined to be imminent. Lin does not operate in such a fashion. Reconsideration of the rejection of claims 16-18 is respectfully requested.

III. Rejection of Claims 3-7 under 35 U.S.C. §103

Claims 3-7 stand rejected under 35 U.S.C. §103 as being rendered obvious by Lin. The Applicants respectfully traverse this rejection.

Claims 3-7 depend directly or indirectly off base claim 1. As such they incorporate the limitations of base claim 1. Lin fails to teach or suggest the detector and the instruction generator that are recited in claim 1. Lin does not disclose an instruction generator that is responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap responsive to the condition that is detected as imminent. Instead, Lin seeks to

perform the speculative spill/fill when processor bandwidth is available to avoid stalling an active process. Thus, Lin teaches away from the claimed invention which requires the execution of steps when the overflow or underflow condition is imminent and thus stalls the active process. Accordingly, the Applicants respectfully urge reconsideration of the rejection of claims 3-7.

IV. Conclusion.

The Applicants have made a good faith effort to place the claims in a state proper for allowance. Should the Examiner feel that a telephone conference with the Applicants' attorney would expedite prosecution of this application, the Examiner is urged to contact the Applicants' attorney at (617) 994-0732.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-023 from which the undersigned is authorized to draw.

Dated: March 1, 2004

Respectfully submitted,

By_____

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